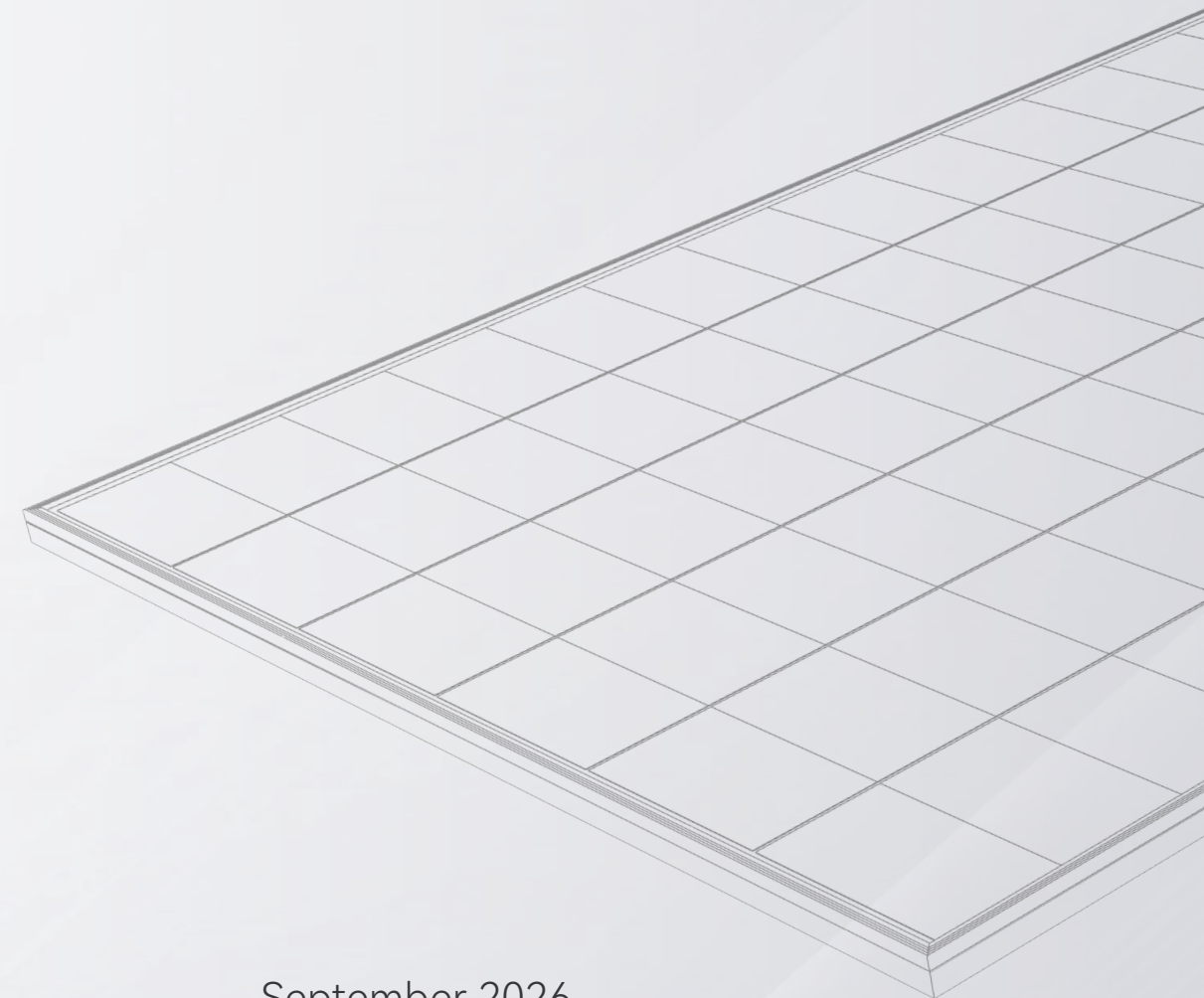


TAC

**Tiger Neo 5.0 Module Platform and Next-Generation Advanced Crystalline Silicon Cell
TAC Technology Whitepaper**



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01 TAC Technology Overview and Development Background

1.1 Technology Development Trends in the PV Industry

The photovoltaic industry has now entered a stage where efficiency leads and systems win. As the TOPCon route approaches its theoretical efficiency limit (~28.7%), the focus of technological competition has shifted from "which single structure is superior" to "how to achieve, on the same silicon wafer, the system-level integration of excellent optical and electrical performance simultaneously."

1.2 TAC Technology Naming and Industry Background

TAC (TOPCon-based Amorphous-Si Passivating Cell) is JinkoSolar's next-generation platform concept built upon the foregoing assessment. Its name directly defines the technology's core:

- **TOPCon-based: A tunnel oxide layer + doped polysilicon (poly-Si passivating contact)** serves as the cell's primary contact system and substrate, inheriting JinkoSolar's N-type TOPCon leadership in manufacturing maturity, supply-chain scale, and patent reserves.
 - **Amorphous-Si Passivating: Intrinsic/doped amorphous silicon (a-Si:H)** heterojunction passivation is introduced at the P-type emitter, reducing the surface recombination velocity to extremely low levels through chemical passivation and delivering a higher open-circuit voltage (Voc).
 - **Cell: Through an interconnection structure**, the two passivating contacts—TOPCon and a-Si:H—are integrated on the rear side of the same wafer, achieving full optical absorption with no front metal shading.
- In short, TAC = "TOPCon substrate + amorphous-silicon passivation enhancement." It unifies the best electrical performance (TOPCon/HJT) with the best optical performance into a single, physically complementary structure: the amorphous-silicon system excels in passivation quality and open-circuit voltage, while the tunnel-oxide system excels in contact resistance and process compatibility. Along this path, TAC further balances performance with mass-production economy, approaching the respective technical ceilings of both routes within a single cell structure and thereby approaching the physical limit of surface recombination velocity. It also reserves a structural interface for subsequent perovskite/TOPCon tandems (lab-certified efficiency already reaching 34.82%, the 33rd world record).

1.3 TAC Technical Principles: Triple Restructuring of Interface, System, and Geometry

TAC builds two complementary passivating contacts on the rear of an N-type wafer: the N-region employs a TOPCon tunnel oxide layer with heavily doped polysilicon to achieve highly selective tunneling transport of electrons; the P-region employs an intrinsic/doped amorphous-silicon heterojunction to achieve chemical passivation and high V_{oc} . The two structures are interleaved on the rear side through high-precision laser patterning and dielectric isolation. TAC performs a triple restructuring—interface, system, and geometry—of existing cell technology.

Interface restructuring: a semiconductor-grade passivating interface. TAC introduces the mature heterojunction interface engineering of the semiconductor industry into an all-back-contact architecture. The P-region builds a hetero-passivating interface with hydrogenated amorphous silicon and a transparent conductive oxide (TCO), integrating chemical passivation, field-effect passivation, and lateral transport; the N-region uses a quantum tunnel oxide layer to achieve low-contact-resistance selective electron transport. Direct metal-silicon contact is structurally eliminated, and the entire electrode area achieves integrated "passivation-selective collection." This enables TAC to combine the high open-circuit voltage of heterojunction technology with the low contact resistance of tunnel-oxide technology, with its efficiency ceiling approaching the theoretical limit of crystalline silicon.

System restructuring: full-stack synergy from cell to module. The generational advantage at the cell level is fully realized through the module technologies of the Tiger Neo 5.0 platform: UMI (Uniform Dot-Matrix Interconnect): Reconstructing the Current Network, GCA (Gapless Cell Array) restructures module density through gapless packaging, and ACC (All-Consistent-Color) restructures the appearance standard with all-black, zero color deviation. Optics, electronics, and aesthetics are unified into one; advancement no longer stays on the cell spec sheet, but is embodied in every module the customer receives.

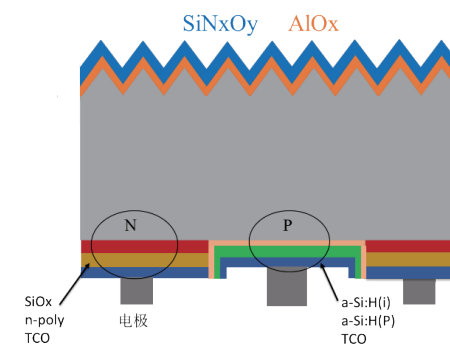


Figure 1. TAC device cross-section: the P-region a-Si/TCO hetero-passivating interface coexists with the N-region quantum tunnel interface

This is not another fine-tuning of moving electrodes to the rear, but a generational restructuring from geometry to core—akin to the leap from a feature phone to a smartphone: the former changed the form, while TAC redefines the core.

1.4 TAC's Generational Leap

The difference between TAC and legacy solutions is not a process tweak within the same architecture, but an overall leap from passivation structure to application positioning. The table below directly presents the generational gap between the two across five dimensions.

Dimension	Legacy solution	TAC
Passivation structure	Single-zone	Dual-zone (2+1 architecture)
Application fit	General-purpose	Exclusive to premium residential
Process route	High-temperature	Low-temperature, low-energy customized process
Efficiency gain	Incremental improvement	Leapfrog breakthrough

From wafer to module: TAC's three-layer architecture

TAC's systematic upgrade comprises a three-layer architecture of "wafer-cell-module": each layer corresponds to a dedicated set of technologies that address three classes of issues—long-term stability, photoelectric conversion, and building aesthetics—and ultimately deliver, on the rooftop, a finished module "exclusive to premium residential."

Layer	Core technology & composition	Core problem solved
Wafer layer	PHS	Long-term stability · Degradation resistance · lifetime longevity
Cell layer	GPP · MCP · FLT · UMI	Recombination loss · Leakage current · Shading resistance · Low-light generation
Module layer	GCA · ACC · PMB	Rooftop color deviation · Visual integration · Installation stability



02 TAC Technology: In-Depth Process Analysis

2.1 TAC Technical Principle

TAC builds two complementary passivating contacts on the rear of an N-type wafer: the N-region employs a TOPCon tunnel oxide layer with doped polysilicon to achieve highly selective tunneling transport of electrons; the P-region employs an intrinsic/doped amorphous-silicon heterojunction to achieve chemical passivation and high Voc. The two structures are interleaved on the rear side through high-precision laser patterning and dielectric isolation.

2.2 Detailed Explanation of TAC's Eight Core Technologies

TAC fuses the two most efficient crystalline-silicon technology routes of today—heterojunction (HJT) and tunnel oxide passivated contact (TOPCon)—into a single all-back-contact architecture, and combines them with the advanced module technologies of the Tiger Neo 5.0 platform to achieve comprehensive generational leadership from cell to module.

The eight technologies underpinning TAC are connected end-to-end along the chains of wafer, interface, transport, optics, and metallization. The following explains, dimension by dimension across the eight core technology dimensions, how TAC (next-generation advanced crystalline-silicon cell) turns "generational leadership" into measurable, verifiable engineering practice. The endpoint of each technology is the realization of customer value—which is precisely why this whitepaper insists on organizing its technical narrative from the customer's perspective.

1 Global Passivation Process (GPP)

[The ultimate solution to break through 28% cell efficiency, approaching the theoretical limit of monocrystalline silicon]

Key metrics: Cell efficiency 28%+ | Passivation coverage: entire electrode area

Technical principle

P-region (hole collection region): A hydrogenated amorphous-silicon (a-Si:H) passivation stack is adopted, supplemented by a TCO transparent conductive oxide film. At the amorphous-silicon/crystalline-silicon interface, chemical passivation (dangling-bond saturation) reduces the surface recombination velocity to extremely low levels, significantly raising the Voc. The entire process can be completed below 200 ° C, with minimal thermal damage; the TCO layer performs the functions of lateral carrier transport and vertical conduction.

N-region (electron collection region): TOPCon employs an ultra-thin silicon dioxide (1–2 nm) plus heavily doped polysilicon passivating contact at the N-type back surface field, using quantum tunneling to achieve highly efficient selective electron transport while blocking holes, ensuring high FF and low Rs, and further reducing the recombination current density.

The combination of these two advanced passivation technologies becomes the Global Passivation Process on Tiger Neo 5.0.

Technical advantages: Surface recombination velocity approaching the theoretical limit supports a high Voc; full-area coverage eliminates leakage channels and raises the parallel resistance; hydrogen passivation repairs micro-defects and improves long-term stability.

JinkoSolar's advantage: With a process reserve of up to 10 years, we can precisely control the thickness uniformity of the amorphous-silicon film as well as the contact resistance between the TCO and the low-temperature silver paste, thereby ensuring passivation quality and the consumption of low-temperature silver paste.

The photovoltaic conversion efficiency of crystalline-silicon solar cells is, to a large extent, limited by carrier recombination losses at the surface and at the metal-electrode contact regions. In conventional diffused-junction cells, the metal electrode is in direct contact with the silicon substrate, forming a high-recombination-velocity contact interface; meanwhile, surface defect states introduced during wafer slicing and processing constitute additional recombination channels. Passivating contact technology introduces a functional thin layer with both passivation and carrier-selectivity between the metal electrode and the silicon substrate, simultaneously suppressing interface-state density and enabling selective carrier collection. It is the core technology of today's high-efficiency crystalline-silicon cells—its essence is to bring the interface engineering of the semiconductor industry into PV cell design.

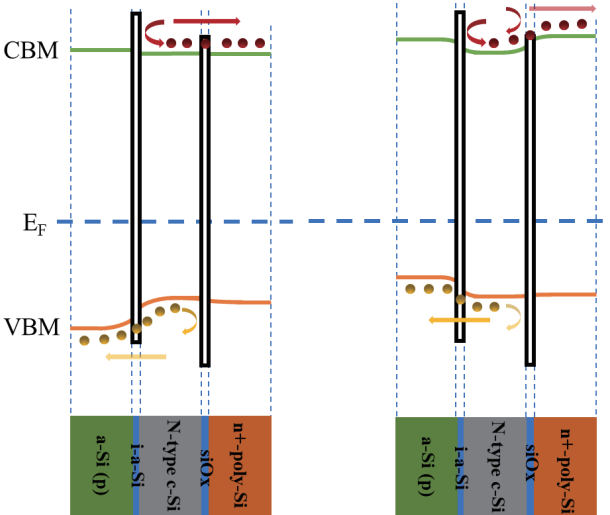


Figure 2. Passivating contact band diagram:
the functional thin layer suppresses interface-state density
and enables selective carrier collection

Compared with existing technology routes, this system achieves upgrades on three levels:

First, an upgrade from local passivating contact to full-area passivating contact. In conventional passivation schemes, the P-region uses P-poly-Si passivation with relatively poor passivation; GPP builds an excellent passivating-contact structure across the entire electrode area of the cell, eliminating poorly passivated regions.

Second, an upgrade from a single high-temperature system to a hybrid high-low temperature system. The P-region adopts a low-temperature amorphous-silicon passivation process while the N-region retains a high-temperature process window; the two regions each use their own optimal process temperature range, avoiding compromise of one region's passivation quality by a single temperature system.

Third, the introduction of TCO material to solve the conductivity bottleneck of the P-region passivating contact. Although the doped amorphous-silicon thin layer offers high passivation quality, its lateral conductivity is low, and direct metallization would introduce contact-resistance loss and recombination loss. The introduction of the TCO layer allows the cell to obtain low contact resistance while maintaining a high open-circuit voltage, achieving synergistic optimization of passivation and contact performance.

This technology choice leverages the advantages of two highly efficient passivation processes to form a complementarity:

The amorphous-silicon passivation system offers advantages in efficiency and low-temperature processing. The core feature of silicon heterojunction (SHJ) technology is the use of a wide-bandgap amorphous-silicon film to electrically isolate the metal electrode from the crystalline-silicon substrate, fundamentally eliminating metal-contact recombination. This mechanism provides excellent interface passivation and, combined with the TCO, effectively reduces contact resistance, endowing the system with a very high open-circuit voltage level. At the same time, the entire SHJ process temperature is below 250 °C, significantly lower than the 800–900 °C high-temperature diffusion steps of conventional diffused-junction cells. The low thermal budget reduces the thermal stress and warpage of the wafer, lowers the breakage rate, and provides process feasibility for wafer thinning.

The tunnel-oxide system offers advantages in compatibility and efficiency ceiling. TOPCon technology features simple fabrication, no light-induced degradation in N-type wafers, and compatibility with conventional high-temperature firing processes, and therefore offers the best mass-production economy. Simulation calculations show that the cell efficiency limit based on the TOPCon structure is closest to the theoretical limit efficiency of crystalline-silicon cells.

2 Multi-Dimensional Charge-Locking Passivation (MCP)

[No edge leakage, no power loss]

Key metrics: 100% passivation coverage of sawn edges | Process: cut-first-then-passivate · in-situ passivation

Electrode passivating contacts solve the recombination problem at the metal-silicon interface, but for half-cut or multi-cut cells there is another, often underestimated, loss mechanism—edge recombination. Modern high-power modules widely adopt half-cut or multi-cut cells to reduce series-resistance loss, making the cutting process a mass-production standard. However, the cutting process also introduces a mechanically damaged layer and unpassivated cross-sections at the cell edges, forming a high-recombination-velocity edge interface. Studies show that edge recombination is a significant loss channel in cells with a large perimeter-to-area ratio and poor edge passivation (such as cut cells and shingled cells), manifesting mainly as declines in fill factor and open-circuit voltage.

JinkoSolar's TAC Multi-Dimensional Charge Passivation technology (MCP 2.0), developed on the basis of JinkoSolar's extensive experience in multi-cut cell engineering and previous sliced-wafer passivation technologies, performs systematic passivation restructuring of the cut edges across four dimensions.

In the conventional process flow, the cell is cut only after all passivation and metallization are completed, so the cut cross-section becomes the only silicon surface in the entire flow that has not undergone any passivation. MCP technology adjusts the process sequence with a "cut-first-then-passivate" scheme: slicing is completed at the front end of cell preparation, while still in the wafer state, so that the cross-section and the wafer surface enter the same passivation step, achieving in-situ edge passivation without an additional post-cut cell-level repair process.

Around the cross-section damage layer, MCP technology implements systematic passivation repair across four dimensions:

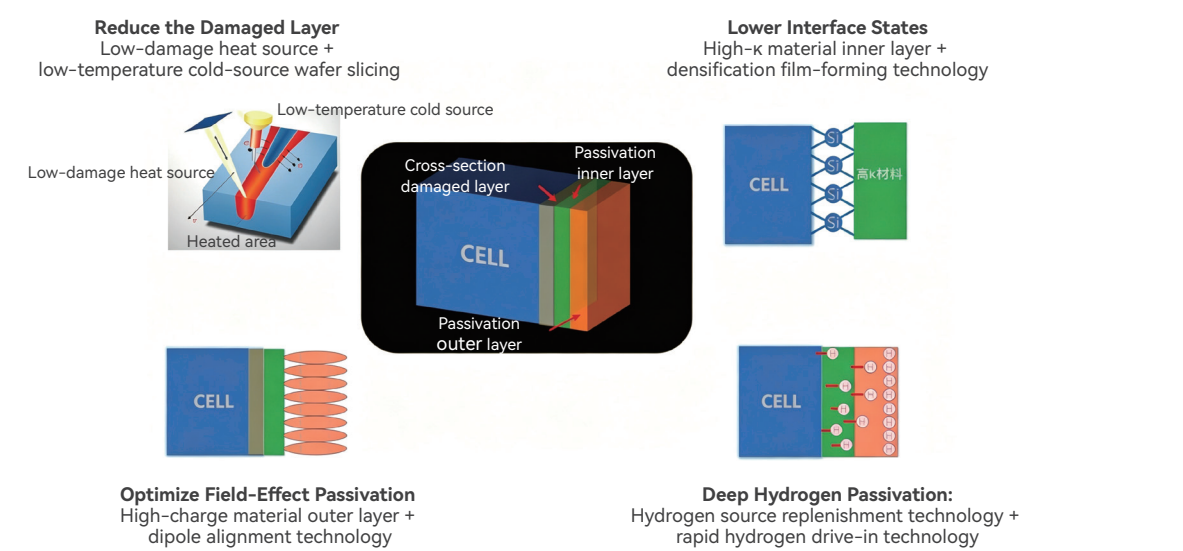


Figure 3. MCP four-dimensional passivation repair: low-damage cutting, chemical passivation, field-effect passivation, and deep hydrogen passivation

Dimension 1 — Low-damage cutting: synergy of a low-damage heat source and a low-temperature cold source. Wafer cutting adopts the principle of thermally induced separation, using a superimposed local laser heat source and cooling source to build a controlled stress field that guides cleavage, reducing the damage-layer depth at the source. Compared with the melting-cut route, this approach "heats only without vaporization," producing no slag, protrusions, or micro-cracks, and providing a low-defect-density initial cross-section for subsequent passivation.

Dimension 2 — Inner passivation layer, chemical passivation: The silicon edge regions exposed after laser cutting are covered by a dense film grown via thermal oxidation. This film effectively wraps the dangling bonds and damaged regions at the cut edge, suppresses edge carrier recombination, reduces leakage-current paths, and at the same time blocks the ingress of moisture and metallic impurities, significantly improving the cell's open-circuit voltage and long-term reliability.

Dimension 3 — Outer passivation layer, field-effect passivation: synergy of high-charge-density material and charge polarity. A dielectric layer with high fixed charge density is built atop the inner layer; the electrostatic field induced by the fixed charge at the silicon surface repels minority carriers, achieving field-effect passivation.

Dimension 4 — Deep hydrogen passivation: hydrogen-source replenishment and rapid hydrogen drive-in. Interstitial hydrogen atoms can bind to various defects in silicon (lattice defects, metallic impurities, laser-induced defects, and surface dangling bonds) and electrically deactivate them. MCP adopts a combined strategy of "hydrogen-source replenishment + rapid hydrogen drive-in": on one hand, it replenishes the hydrogen reservoir in the dielectric stack; on the other, it uses a rapid thermal process to regulate the charge-state distribution and injection depth of hydrogen, accelerating hydrogen transport toward the cross-section damage layer and eliminating edge recombination centers.

MCP and GPP form a complementary dual-passivation architecture: GPP solves the recombination problem at the electrode-contact region, while MCP extends the passivation boundary from the electrode to the cut cross-section. The technical path corresponds to the complete chain of "reduce damage introduction—chemical passivation—field-effect passivation—defect hydrogen passivation," turning the cut edge into a controlled interface at the same level as the main passivation surface.

Customer value | Villa roofs have multiple orientations, with skylights and chimneys; the multi-cut design is key to improving layout adaptability. But in conventional processes, the finer the cell is cut, the more severe the edge leakage, and the gains that should have been obtained are eaten up by the process itself. TAC is the opposite—the cross-section is fully passivated by semiconductor-grade processing, and the finer the cut and the higher the density, the more fully the power advantage is released. Every watt generated by the cell is delivered completely to the module output terminal, without being lost to cutting.

3 Full-Spectrum Light Trapping (FLT)

[From dawn to dusk, from rain to shine — generating around the clock, wasting no light]

Key metrics: Front metal shading approaching 0 | Infrared optical path multiplied | Wide incidence-angle response

Technical principle: Through the synergy of the anti-reflection coating stack, the surface texturing, the rear high-reflection dielectric, and the gap reflective film, the photon absorption path is maximized and long-wavelength secondary absorption is enhanced. JinkoSolar names this the Full-Spectrum Light Trapping (FLT) structure on Tiger Neo 5.0; the platform-level FP (multi-cut cell technology) increases module power by about 10 W by reducing I^2R loss, improving heat dissipation, and lowering shading loss.

Process principle: Alkaline texturing or nano-imprinted inverted-pyramid texturing + dual-layer $\text{SiN}_x/\text{Al}_2\text{O}_3$ anti-reflection coating; a rear gap reflective film reflects transmitted light back to the cell; FP multi-cut cells achieve low-loss reconfiguration of the current path.

Technical advantages: Raises the short-circuit current I_{sc} and reduces optical loss; long-wavelength reuse increases energy yield; combined with the front shading-free BC design, optical gain is maximized; FP multi-cut cells simultaneously improve heat dissipation and shading resistance.

JinkoSolar's advantage: We can ensure the matching of the film stack at different incidence angles; we minimize the impact of texturing on passivation-layer uniformity, guaranteeing the long-term stability of the anti-reflection coating under UV aging; and we balance rear reflectance against rear shading.

Light trapping is one of the most fundamental optical-gain mechanisms in crystalline-silicon photovoltaics. Crystalline silicon is an indirect-bandgap semiconductor with a very low absorption coefficient for near-band-edge infrared photons ($\approx 900\text{--}1200\text{ nm}$); a single pass through the wafer is insufficient for effective absorption. A light-trapping structure, through the combination of surface texturing and rear reflection, causes weakly absorbed light to undergo multiple total internal reflections inside the wafer, repeatedly folding back to extend the optical path.

To maximize the use of the light-trapping effect, FLT technology adopts integrated optical-path control, systematically designing from front-side light incidence and rear-side reflection to surface texturing.

The front light-incidence interface is "transparent." Relying on the all-back-contact architecture, both positive and negative electrodes are transferred to the rear; the front light-incidence interface has no busbar or finger shading, and front metal shading loss approaches zero.

Rear infrared reflection layer. An infrared high-reflection layer is introduced on the rear, reflecting unabsorbed near-band-edge photons back to the wafer and scattering them into large-angle paths, extending the penetration path of weakly absorbed infrared photons and enhancing crystalline silicon's photon absorption and current-conversion capability in the infrared band.

Multi-dimensional light-path control (MLC) and SSI composite texturing. Conventional single-scale texturing suffers significantly degraded anti-reflection performance under oblique incidence, and mirror-like rear reflection struggles to confine long-wavelength photons. Through the combination of multi-dimensional light-path control and SSI composite texturing, FLT simultaneously achieves, over a wide incidence-angle and wide-spectrum range: front composite texturing reduces interface reflection at different incidence angles; rear scattering reflection breaks the specular escape channel, allowing incident light of different angles and wavelengths to enter the multiple-fold light-trapping cycle. As a result, oblique morning and evening light and overcast diffuse light are no longer largely lost, and the industry pain point of low utilization of weak and oblique light is systematically improved.

Customer value | A family's peak electricity demand is in the early morning and evening—precisely the time when traditional modules generate the least, so the power generated cannot be used and the power needed cannot be generated. TAC makes the generation curve wider and flatter: from dawn to dusk, from rain to shine, with the same installed capacity, it harvests more real energy over the year and better matches the real rhythm of life. Every time the generation curve approaches the household load curve is one more kilowatt-hour saved on the bill.

4 Premium Homogeneous Silicon Substrate (PHS)

[Every wafer carries an ID card — a good cell starts with a good wafer]

Key metrics: Wafer-level full-process quality traceability | High purity · Homogeneity · Low defects · Low oxygen

Technical principle: TAC uses N-type Czochralski monocrystalline silicon as the substrate and imposes stricter requirements on metallic impurities, oxygen and carbon content, and native crystal defects than conventional TOPCon, ensuring a bulk minority-carrier lifetime $> 2\text{ ms}$ and a bulk recombination current density $J_{0,bulk} < 5\text{ fA/cm}^2$, providing a high-quality carrier foundation for the subsequent stacking of amorphous-silicon passivation and tunnel contact. This substrate has been designated by JinkoSolar as a core process element of Tiger Neo 5.0.

Process principle: High-purity polysilicon feedstock $\rightarrow$ Czochralski crystal pulling (CCz/RCz) $\rightarrow$ diamond-wire sawing $\rightarrow$ wafer gettering $\rightarrow$ minority-carrier-lifetime and resistivity sorting; the crystal-pulling stage suppresses impurity segregation through thermal-zone optimization.

Technical advantages: Reducing bulk recombination at the source is the physical prerequisite for breaking through 28% efficiency; a high minority-carrier lifetime improves the defect tolerance of subsequent passivation layers; a homogeneous substrate reduces power-distribution dispersion and improves string consistency.

JinkoSolar's advantage: Intrinsic control of native micro-defects (B-O complexes, thermal donors); maintaining the uniformity of the wafering damage layer and the lateral resistivity uniformity of large-format (182/210 mm) wafers; and balancing the cost of high-purity feedstock against crystal-pulling yield.

The wafer is the core of the module; wafer quality directly determines module efficiency and reliability. Tiger Neo 5.0 / TAC adopts the Premium Homogeneous Silicon Substrate, upgrading wafer quality comprehensively through four key technologies:

First, Intelligent Doping Uniformity (IDU). Relying on AI-assisted precise doping control, it suppresses the axial resistivity drift caused by the segregation effect during crystal pulling, achieving both intra-wafer and inter-wafer resistivity homogeneity. Improved resistivity uniformity brings two benefits: first, the cell-efficiency distribution narrows and the share of high-efficiency bins rises [20]; second, consistency of cell operating points at the module end improves, reducing within-string mismatch loss and bright/dark-cell differences.

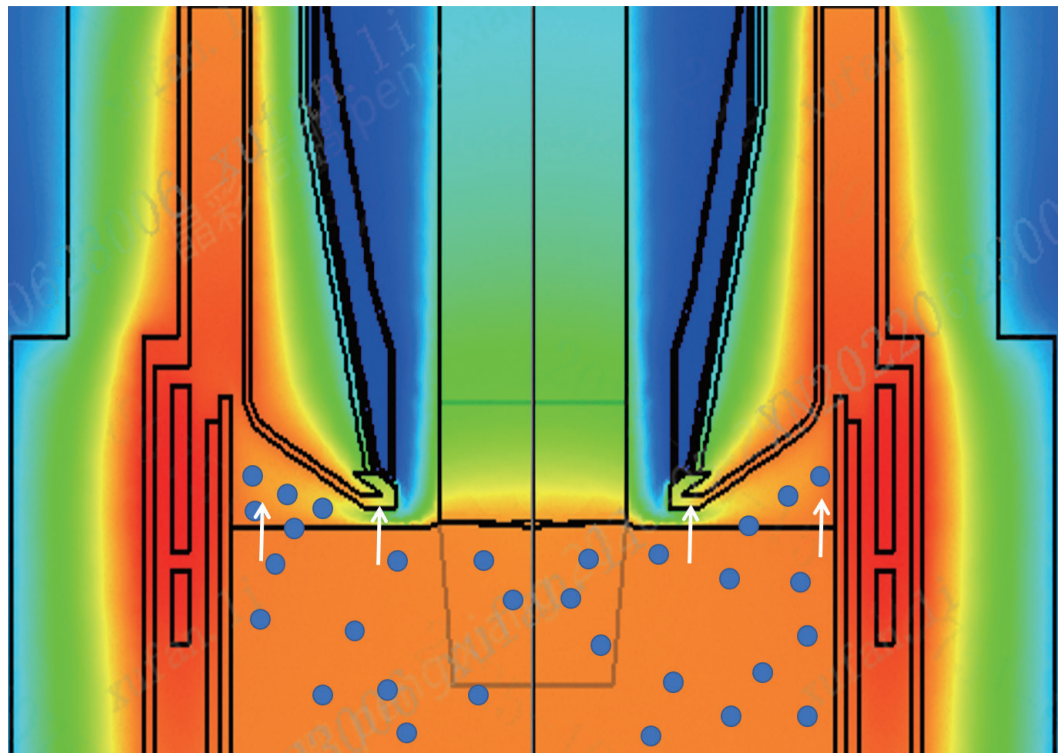


Figure 5. IDU intelligent doping uniformity simulation

Second, Defect Suppression Enhancement (DSE). Through defect-control engineering covering the entire crystal-growth and thermal-processing flow, it suppresses the formation and development of dislocations and micro-defects, improving the wafer's minority-carrier lifetime .

Third, Wafer Quality Traceability (WQT). Wafer-level full-process inspection and data traceability are implemented, building a dedicated record for each wafer covering the quality parameters of crystal pulling, cropping, and slicing, enabling full-process query of quality parameters and precise interception of anomalous wafers, and guaranteeing the consistency and traceability of production batches.

Fourth, Ultra-Low Oxygen Fabrication (ULO). A low-power oxygen-reduction hot zone is adopted to lower the interstitial oxygen content of the crystal. Oxygen is the highest-concentration impurity in Czochralski silicon; for N-type wafers, its harm lies in the strong recombination activity of oxygen-related defects such as oxygen precipitates formed during high-temperature processes (e.g., boron diffusion). Lowering the oxygen content effectively improves the long-term stability of the module.

The stacking of the four technologies gives TAC wafers the core advantages of high purity, high homogeneity, low defects, and low oxygen content.

5 Uniform Matrix Interconnection (UMI)

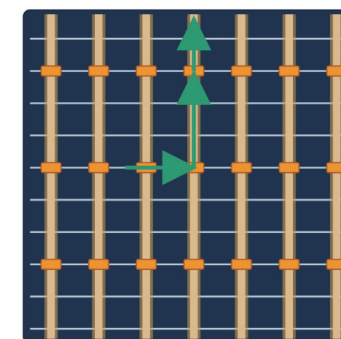
[No main road — only expressways]

Key metrics: 0 busbars | distributed dot-matrix extraction | shortened current path

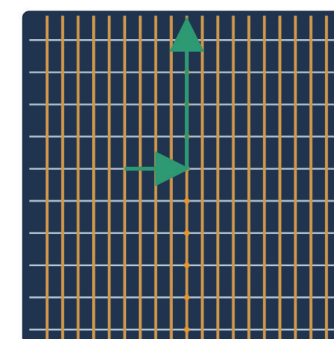
Technical principle: TAC adopts UMI technology, eliminating printed busbars on the cell; current is extracted distributively through the alloy dot matrix to the ribbon, shortening the current path by two stages and substantially reducing ohmic loss. Paired with a low-stress interconnection technology, it markedly lowers the peak soldering temperature and thermal stress, thereby removing the thermal stress of high-temperature soldering.

Technical advantages: a shortened current-transmission path and lower ohmic loss raise the fill factor and power in tandem; high-temperature soldering thermal stress is eliminated, reducing thermal-shock and hidden-crack risk; silver-paste consumption drops, balancing performance with mass-production economy.

JinkoSolar's advantage: built on the Tiger Neo 5.0 platform's full-process control over UMI layout, curing, and string-welding equipment, it ensures the uniformity and long-term reliability of the uniform dot-matrix interconnect channels; under the back-contact architecture, the seamless interface between UMI and the all-back-surface electrodes reflects JinkoSolar's engineering heritage of advancing UMI from front-side symmetric interconnection to back-side distributed interconnection.



Conventional cell current path



Uniform dot-matrix (UMI) cell current path

Conventional cell current path — four stages: fingers (collect current) → busbar → PAD → ribbon (route current out)

Uniform dot-matrix (UMI) cell current path — two stages: fingers (collect current) → ribbon (route current out)

6 Gapless Cell Array (GCA)

[Highest cell coverage ratio — a true edge-to-edge all-screen]

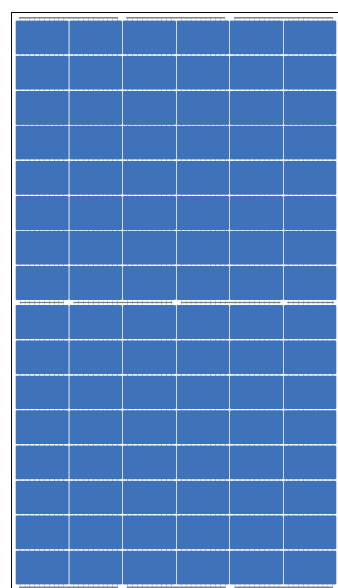
Key metrics: negative cell gap | ribbon fully hidden

Technical principle: leveraging the TAC all-back-electrode architecture, interconnect ribbons no longer need to cross the cell front, creating the structural prerequisite for a negative cell gap; through back-side distributed inter-connection and low-stress encapsulation, the ribbon on both sides of the cells and at the module center in conventional modules are fully hidden, and together with the MCP passivate-after-cut process that guarantees cut-edge quality, high-density packaging with a negative cell gap is achieved.

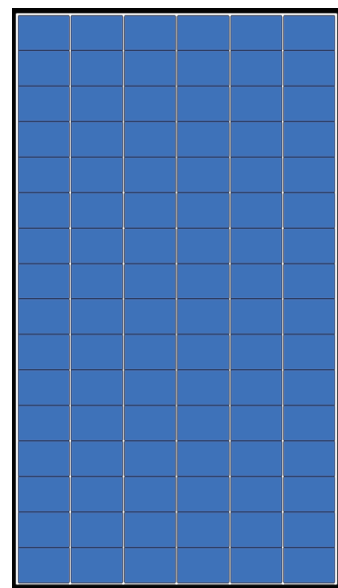
Technical advantages: GCA (Gapless Cell Array) substantially eliminates non-generating area, increasing the effective light-receiving area of cells within the module by 2% and raising module power by 10 W.

JinkoSolar's advantage: drawing on JinkoSolar's systematic engineering accumulation across interconnection methods, encapsulation stress control, and cut-edge quality, GCA is brought from concept to a mass-producible, verifiable encapsulation process.

Customer value: roof area is irreversibly limited, and every square meter must generate. GCA converts the area wasted on cell gaps and ribbon entirely into light-receiving area — at the same roof size, more generating capacity is packed in, generating more power without moving a single tile.



Conventional module



TAC module

The upper, middle, and lower ribbons and cell gaps of a conventional module are all concealed in TAC, with zero cell gap

7 All-Black Zero Color-Deviation (ACC)

[Black — truly black]

Key metrics: Cell-encapsulant-frame uniformly colored across the chain

As a product built for residential applications, TAC's design for aesthetics is embodied in its all-black aesthetics. Technically, it rests mainly on three aspects:

First, precise control of film deposition. The apparent color of a cell is not an intrinsic material property but is determined by the interference effect of the passivation/anti-reflection film stack. When the film thickness deviates from the design value, the wavelength of destructive interference drifts accordingly, and the apparent cell color changes detectably—this is also the main source of color deviation in mass-produced cells. In other words, the essence of color-deviation control is inter-wafer consistency control of film thickness and refractive index. ACC technology applies finer control of thickness and refractive index to the passivation films, compresses the inter-wafer distribution of the film stack's optical parameters, narrows the color-distribution bandwidth at the source, and keeps the color-deviation distribution within the human-eye perceptible threshold, achieving uniform all-black cells.

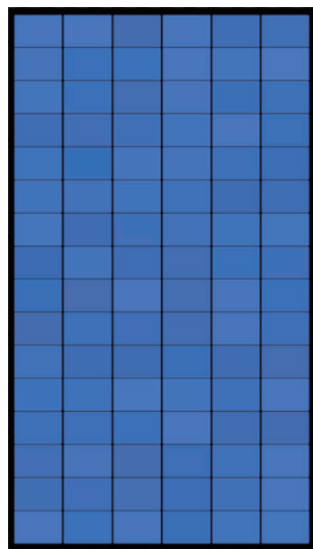
Second, AI-assisted cell sorting. On top of the above process control, image-based AI sorting is introduced: each cell's appearance is imaged and algorithmically graded, and only cells with consistent color-deviation parameters are matched into a module. AI sorting achieves fully automatic visual screening of cells, preventing discrete off-color cells from entering.

Third, color coordination of auxiliary materials. Module-level "all-black" depends on more than the cells: inconsistent colors of the encapsulant film, ribbons, and frame create visual breaks. ACC applies color-coordinated design to auxiliary materials such as the encapsulant, making the chromaticity of cells, encapsulant, and frame consistent, and achieving an overall "true all-black" appearance from cell to module.

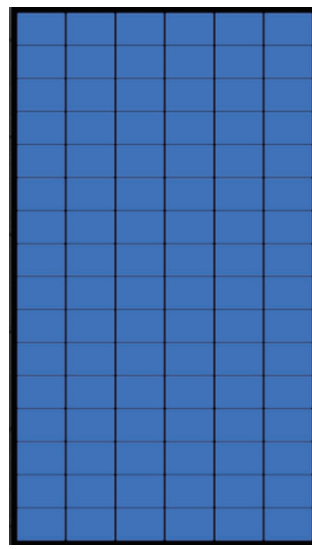
Technical advantages: inter-cell color deviation falls below the human-eye perceivable threshold, achieving visually colorless deviation; the front-side grid-free design provides the structural prerequisite for an all-black aesthetic — with no silver grids, the all-black appearance blends seamlessly with dark tile roofs.

JinkoSolar's advantage: leveraging the Tiger Neo 5.0 platform's process control over film thickness and refractive index, together with fully automated AI visual sorting, JinkoSolar achieves full-chain color consistency from cell to module and batch uniformity — reflecting its integration of "aesthetics" into the mass-production quality system.

Customer value: a house is the most expensive asset, and its appearance must not be compromised. ACC (All-Black Zero Color-Deviation) makes the module appear, viewed from the street, as only the roof — not the modules — blending seamlessly with dark tile roofs.



Conventional process



ACC zero color deviation

8 Perimeter Moisture Barrier (PMB)

[Every edge and corner, fully covered]

Key metrics: Solid-state insulation | Edge sealing stable across the full lifecycle

Technical principle: butyl rubber (Butyl) is applied around the module perimeter to form a continuous edge seal; leveraging its intrinsic advantage of reducing the water vapor transmission rate (WVTR) by more than 60% versus conventional encapsulant films, it ensures long-lasting water blocking and long-term reliability.

Technical advantages: a continuous, dense water-blocking barrier is built around the module perimeter, blocking moisture and corrosive media from infiltrating inward along the edge at the source; it also provides excellent electrical insulation, serving as edge-insulation supplementation that suppresses leakage-current and surface-discharge risk under wet conditions; across a wide temperature range it retains elasticity and adhesion, absorbing and buffering the interfacial deformation stress from thermal cycling and mechanical load, lowering the probability of delamination and edge hidden cracks, and safeguarding the integrity of the sealing interface over long-term service.

JinkoSolar's advantage: with the Tiger Neo 5.0 platform's stringent PMB (Butyl edge sealing) process control, JinkoSolar has elevated edge sealing from a "module-level auxiliary material" to a critical link in "cell-to-module full-lifecycle reliability design."

Customer value: "install it and stop worrying." The value of residential modules lies in "long-term maintenance-free" operation, and the edge is precisely the weakest link where moisture ingress triggers corrosion, delamination, and insulation degradation. Through the material's intrinsic insulation and water resistance, PMB (Butyl edge sealing) turns "invisible safety" into a verifiable promise — for greater peace of mind over 40 years.

03 TAC Module Core Advantages

3.1 High-Efficiency TAC Cells and Cross-Generational Module Efficiency

TAC's maximum cell efficiency reaches 28%, approaching the theoretical limit of monocrystalline-silicon cells. At the module level, combining module-level zero-gap layout with concealed-ribbon technology, TAC's module efficiency exceeds 25.52%, the highest mass-production efficiency in the industry, with the same-format module delivering about 10–15 W more power than BC.

The zero-gap layout converts the originally non-generating blank area between cells into a generating area by eliminating the ineffective gaps; the concealed ribbons move the ribbons to the rear, further releasing front light-receiving area. Together with front zero-shading, the two jointly support TAC's cross-generational efficiency leap at the module level.

3.2 TAC Module Low-Irradiance Response

Relying on TOPCon's low-leakage-current characteristic and parallel-resistance optimization, TAC maintains 95%–98% relative power even in the 100–200 W/m² low-irradiance range, The higher current-collection efficiency under low irradiance makes the "shoulders" of the generation curve fuller in mornings, evenings, and rainy days.

3.3 TAC Module UV-Degradation Resistance

In UV-induced degradation (UVID) testing, the inherited TOPCon structure of TAC outperforms BC, whereas the TOPCon system keeps UV degradation within 2%. The excellent UVID resistance stems from the passivation layer's effective suppression of UV-induced defects.

3.4 TAC's Structural Advantages over BC

Beyond efficiency and energy yield, TAC also differs from BC at the levels of semiconductor structure and engineering reliability, mainly in two aspects.

- **Passivation system:** BC still relies on a single PERC or TOPCon homojunction and passivating-contact system; TAC integrates two systems on the same wafer—amorphous-silicon heterojunction chemical passivation and TOPCon tunnel passivating contact—achieving optimal passivation in the P-region and N-region respectively, representing a systemic breakthrough at the semiconductor level.
- **Interconnection reliability:** BC is prone to warpage because its fully back-contact grid lines are heated collectively; the adoption of low-stress interconnection technology significantly reduces the peak soldering temperature and thermal stress, suppressing warpage and hidden cracks at the source and minimizing thermal damage to the cell passivation structure and metallization, while also accommodating wafer thinning to enable low-stress, reliable interconnection of the back-contact grid lines. Inheriting the TOPCon base, TAC exhibits a more uniform grid-line stress distribution, validated across an installed base exceeding 1000 GW.

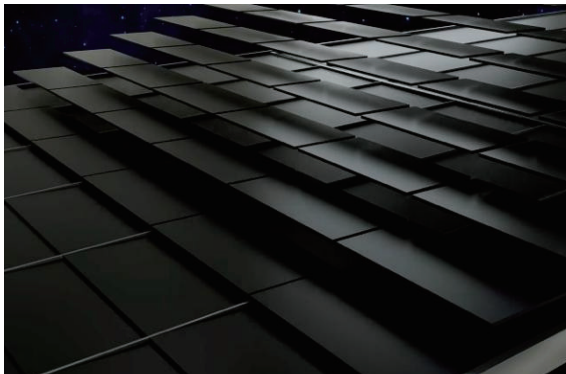
04 TAC Technology: Long-Term Sustainability

4.1 Invisible Gridline Technology

Uniform Dot-Matrix Interconnect (UMI) technology reduces shading and resistive losses, delivering a cell-efficiency gain of 0.3%–0.5%, and represents one of the near-to-mid-term pathways for advancing TAC toward 28%+.

Reliability considerations:

Busbar-free interconnection demands extremely high soldering alignment accuracy and requires high-precision positioning, low-stress soldering, and pull-force monitoring to ensure contact stability under 25–30 years of mechanical fatigue.



4.2 Low-Temperature Cell Technology

TAC's a-Si passivation region inherently adopts a low-temperature process below 200 ° C, is naturally compatible with low-temperature metallization, reduces thermal stress and micro-crack risk, and opens room for wafer thinning.

Reliability considerations:

For copper-containing schemes (silver-coated copper / copper electroplating), the long-term oxidation-resistance and copper-diffusion risks must be addressed, and scaled adoption may proceed only after cross-cycle validation.

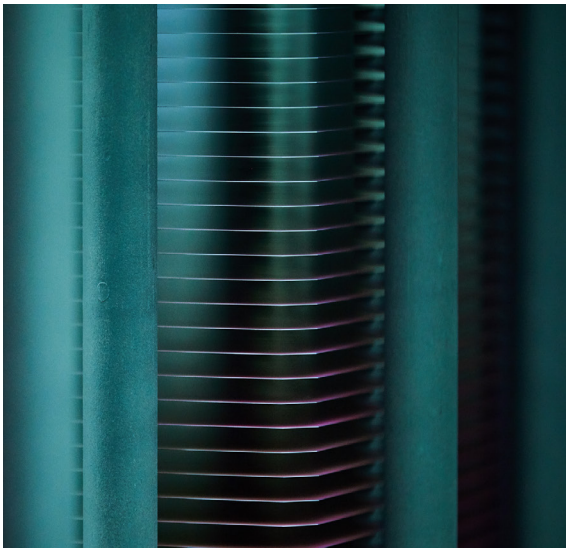


4.3 Tandem Cells

Once single-junction crystalline silicon approaches its limit, the "tunnel oxide layer + amorphous passivation + full rear interconnection" structure established by TAC can directly serve as the bottom-cell platform for perovskite tandems. JinkoSolar's perovskite tandem cell based on N-type TOPCon has achieved a lab-certified efficiency of 34.82% (the 33rd world record), reserving a clear interface for TAC's evolution toward next-generation form factors.

Reliability considerations:

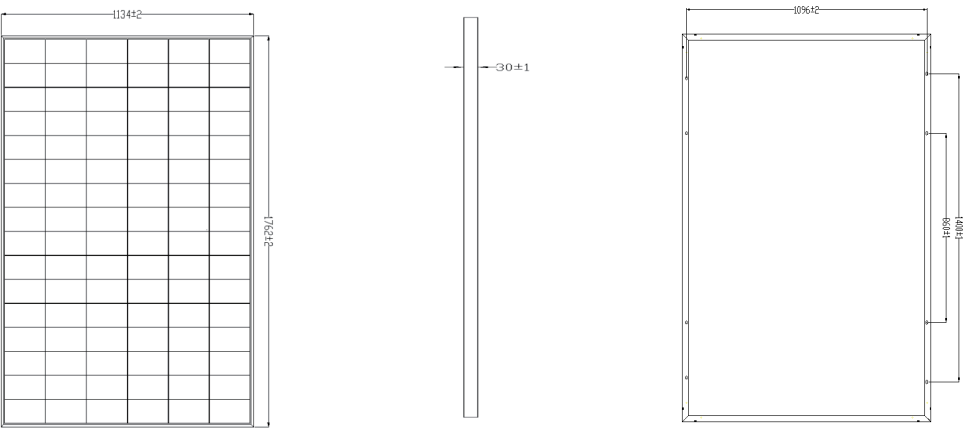
The stability of perovskites (damp-heat, light degradation) and large-area uniform fabrication remain core industrialization challenges; tandem commercialization is still expected to take several years.



05 TAC Technology: Product Applications

Product Parameter Overview

Translating every technology into a single line on the specification sheet. This chapter focuses on the core highlight parameters of the TAC residential module (Standard Test Conditions, STC). The complete parameters are subject to the official product datasheet released by JinkoSolar.



Parameter	Value
Module type	Tiger Neo 5.0 TAC (JKM485-510T)
Module configuration	All-Black Monofacial · Dual-Glass module
Cell technology	TAC (tunnel-oxide / amorphous-silicon composite passivated cell, N-type monocrystalline)
Maximum power Pmax	Up to 510 W
Module efficiency	Up to 25.52%
Module dimensions	1762 × 1134 × 30 mm
Weight	22.0 kg
Power temperature coefficient (Pmax)	−0.24 %/°C
Product warranty / Linear power warranty	Lifetime warranty service(see warranty manual for detailed terms)
Operating temperature	−40 ~ +70 °C

06

TAC Technology: Customer Value

Module Application Value

Illustrative Owner Benefit Assessment (Detached House in Europe: Netherlands / Germany)

The table below compares key indicators of TAC and a conventional 480 W residential module under the same roof scenario, assuming a 40-year comparison period:

Metric	TAC 510W	Conventional 480W (representative baseline)	Advantage
Peak power per module	510 W	480 W	+30 W (+6.25%)
Power density per unit area	255 W/m ²	240 W/m ²	+15 W/m ²
Deployable on 50 m ² roof	~24 modules / 12.24 kW	~24 modules / 11.52 kW	+0.72 kW
Power temperature coefficient (Pmax)	-0.24 %/°C	-0.26 %/°C	Less degradation under high temperature
Annual equivalent full-load hours	1,050 kWh/kWp	1,050 kWh/kWp	Depends on regional resource conditions
First-year energy yield	12,884 kWh	12,000 kWh	+884 kWh
40-year cumulative energy yield	500,015 kWh	428,640 kWh	+71,375 kWh
40-year incremental discounted benefit	—	—	+13,419 EUR
Discounted LCOE (5%)	0.097 EUR/kWh	0.099 EUR/kWh	Lower
Payback period of incremental system cost	—	—	~7.5 years

- **Location:** A typical detached house in Europe (Netherlands/Germany as examples, 51°–52° N, moderate solar resource).
- **Available roof:** 50 m² (main north-/south-facing roof, net installable area after deducting ridge, setback, and maintenance access).
- **Annual equivalent full-load hours:** 1,050 kWh/kWp (AC side, including system losses, PR≈0.85).
- **Degradation:** 1.0% in the first year, then 0.30%/year linear for TAC and 0.40%/year for the conventional case.
- **Electricity price (EUR):** retail 0.35/kWh (taxes included), 40% self-consumption, 0.08/kWh for surplus feed-in.
- **System cost:** 1.50 EUR/W all-inclusive (module + BOS + labor, including typical local subsidies), same basis for both; O&M 0.010 EUR/W/year; discount rate 5%.
- The "conventional 480 W" baseline represents typical parameters of mainstream 2025 residential modules (temperature coefficient and warranty taken as typical values for this product class), not a specific brand; actual values vary by product.
- **Currency:** EUR.



For the same 50 m² roof, TAC's higher power density per unit area (255 vs 240 W/m²) allows about 0.72 kW more installed capacity, and combined with its better temperature coefficient, yields about 884 kWh more in the first year; as the conventional case degrades faster, this gap widens further to about 71.4×10³ kWh cumulatively over 40 years. At the local residential electricity price, the incremental generation is worth about 314 EUR per year, with a 40-year cumulative discounted benefit of about 13,419 EUR (excluding electricity-price increases). The discounted levelized cost of energy (LCOE, 5% discount rate) for TAC is about 0.097 EUR/kWh, lower than the conventional 0.099 EUR/kWh; because the roof area is fixed and TAC's per-area output is higher, the additional system cost versus the conventional case can be recovered in about 7.5 years, after which it is net gain. This calculation illustrates the relative gain under a single-roof scenario; actual benefits vary with location, electricity price, shading, and system configuration.

Illustrative Owner Benefit Assessment (Detached House in Australia)

The table below compares key indicators of TAC and a conventional 480 W residential module under the same roof scenario, assuming a 40-year comparison period:

Metric	TAC 510W	Conventional 480W (representative baseline)	Advantage
Peak power per module	510 W	480 W	+30 W (+6.25%)
Power density per unit area	255 W/m ²	240 W/m ²	+15 W/m ²
Deployable on 50 m ² roof	~24 modules / 12.24 kW	~24 modules / 11.52 kW	+0.72 kW
Power temperature coefficient (Pmax)	-0.24 %/°C	-0.26 %/°C	Less degradation under high temperature
Annual equivalent full-load hours	1,500 kWh/kWp	1,500 kWh/kWp	Depends on regional resource conditions
First-year energy yield	18,433 kWh	17,144 kWh	+1,289 kWh
40-year cumulative energy yield	715,448 kWh	612,343 kWh	+103,105 kWh (+16.8%)
40-year incremental discounted benefit	—	—	+19,074 AUD
Discounted LCOE (5%)	0.050 AUD/kWh	0.051 AUD/kWh	Lower
Payback period of incremental system cost	—	—	~3.8 years

- **Location:** A typical detached house in Australia (represented by the Sydney metropolitan area, 34° S, excellent solar resource).
- **Available roof:** 50 m² (main north-/south-facing roof, net installable area after deducting ridge, setback, and maintenance access).
- **Annual equivalent full-load hours:** 1,500 kWh/kWp (AC side, including system losses, PR≈0.85).
- **Degradation:** 1.0% in the first year, then 0.30%/year linear for TAC and 0.40%/year for the conventional case.

- **Electricity price (AUD):** retail 0.38/kWh (taxes included), 35% self-consumption, 0.08/kWh for surplus feed-in.
- **System cost:** 1.10 AUD/W all-inclusive (module + BOS + labor, including typical local subsidies), same basis for both; O&M 0.008 AUD/W/year; discount rate 5%.
- The "conventional 480 W" baseline represents typical parameters of mainstream 2025 residential modules (temperature coefficient and warranty taken as typical values for this product class), not a specific brand; actual values vary by product.
- **Currency:** AUD.



For the same 50 m² roof, TAC's higher power density per unit area (255 vs 224 W/m²) allows about 0.72 kW more installed capacity, and combined with its better temperature coefficient, yields about 2,416 kWh more in the first year; as the conventional case degrades faster, this gap widens further to about 103.1×10³ kWh cumulatively over 40 years. At the local residential electricity price, the incremental generation is worth about 447 AUD per year, with a 40-year cumulative discounted benefit of about 19,074 AUD (excluding electricity-price increases). The discounted LCOE (5% discount rate) for TAC is about 0.050 AUD/kWh, lower than the conventional 0.051 AUD/kWh; because the roof area is fixed and TAC's per-area output is higher, the additional system cost versus the conventional case can be recovered in about 3.8 years, after which it is net gain. This calculation illustrates the relative gain under a single-roof scenario; actual benefits vary with location, electricity price, shading, and system configuration.

08 Conclusion

Packing the interface engineering of the semiconductor industry onto the roof of every home.

Every efficiency leap in photovoltaics originates from re-answering "where is the loss." Moving the electrodes to the rear of the cell answered the "front shading" problem; TAC further answers two problems—"rear interface recombination" and "module-end loss"—by eliminating direct metal-silicon contact with a semiconductor-grade hetero-passivating interface and achieving low-resistance electron collection with a quantum tunnel layer, then translating the cell-level generational advantage into a tangible product on the roof through module technologies such as 0BB, GCA, and ACC. TAC's generational nature lies not in following an existing route, but in moving from geometric restructuring to interface restructuring and system restructuring.

The destination of technological progress is the real use scenario. This whitepaper starts from the four demands of detached-house owners in Europe and America: roof area is irreversibly limited, appearance is constrained by community covenants, safety must meet the insulation-coordination requirements of IEC 61730-1:2023, and generation must track the household's real load curve. When efficiency becomes the only lever to move total energy yield, and when "can it be installed" precedes "how much to install," the meaning of advanced technology no longer rests on laboratory parameters, but on whether it can simultaneously deliver more power, more stable safety, and purer aesthetics on the same inch of roof. TAC's eight core technologies are organized precisely around this set of residential-specific constraints: from PHS wafer traceability to GPP global passivation, from MCP edge charge-locking to FLT full-spectrum light trapping, and then to GCA gapless packaging, 0BB distributed interconnection, and ACC zero-color-deviation all-black—each layer and each item corresponds to a concrete rooftop problem.

On the Tiger Neo 5.0 platform, TAC integrates the above capabilities into a residential module "exclusive to premium homes": cell efficiency breaking 28%, per-module power about 30 W higher than the previous generation, and a lifetime product warranty commitment answering the lifecycle expectation of a residential system that is "installed and then left alone." Looking ahead, as hetero-passivating interfaces and tunnel-collection processes mature further, the efficiency ceiling of the all-back-contact architecture still converges toward the theoretical limit of crystalline silicon; yet what truly determines the value of this technology is whether it can continuously translate the precision of semiconductors into quiet, long-lasting, and good-looking generation on the roofs of countless homes. This is precisely the significance of TAC as a generation of technology, not merely an improvement.

For villa owners, TAC means three things: the same roof, more power generated—per-module power about 30 W higher than the previous generation and module efficiency breaking 25.5%, squeezing the roof's value to the limit without adding a single brick or tile; the same house, a more dignified appearance—zero-color-deviation all-black blends seamlessly with the roof, removing one obstacle from community covenants; the same installation, longer peace of mind—lifetime warranty service and solid-state insulated edges turn "invisible safety" into a verifiable commitment. Technology is complex; on the roof it boils down to "generate more, look cleaner, last longer."

